



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,886	08/24/2001	Mukesh K. Patel	032481-034	3543
8791	7590	12/14/2004	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			DAS, CHAMELI	
			ART UNIT	PAPER NUMBER
			2122	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,886	MUKESH K. PATEL 	
	Examiner	Art Unit	
	CHAMELI C DAS	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 506-557,559-607 and 609-615 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 506-557,559-607 and 609-615 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/9/04</u> | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED DESCRIPTION

1. This action is in response to the RCE filed on 10/1/20004.
2. Claims 506-557, 559-607, 609-615 are pending.
3. Claims 558 and 608 have been canceled.
4. Claims 610-615 have been added.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 506-517, 519-546, 548 557, 559-570, 572-594, 595-607, 609-613 are rejected under 35 U.S.C. 102(e) as being anticipated by Tremblay et al, (Tremblay), US 6,125,439.

As per claim 506, Tremblay (US 6,125,439) discloses:

- a method for processing instructions in a central processing unit capable of executing instructions of a plurality of instruction set (Abstract), the processor is the central processing unit is shown in (col 5, lines 43-45)
- including a stack-based instruction (Abstract, lines 1-3) where “hardware processor” is the “stack-based instruction” (col 3, lines 53-56) and a register-based instruction (col 17, lines 32-39), where “stack cache” is register file (col 17, lines 11-16) and the instructions are in stack-cache is the register-based instruction
- maintaining data for register-based instruction from the register-based instruction set (col 3, line 64), where “operations on data are performed through the stack cache”, inherently including maintaining data for register-based instruction as claimed
- operand stack for a operands associated with stack-based instructions ... overflow and underflow mechanism (col 18, lines 29-57, col 17, lines 10-15)
- maintaining an indication of a depth of the operand stack (col 9, lines 20-25), where “an instruction **push this pointer onto operand stack**” inherently including maintaining an indication of a depth of the operand stack as claimed
- executing the stack-based instructions and register-based instruction in an execution unit (abstract)
- including generating an exception in respect of selected stack-based instruction (col 3, lines 39-42).

For claim 507, (col 9, lines 55-58).

For claim 508, (col 3, lines 60-65).

For claims 509, 562, 563, 564 (col 9, lines 55-57, col 11 lines 7, col 17, line20, line 30), all the stack caches are denoted by the number 155, shows that first, second and third register files are the same register file.

For claim 510 (col 18, lines 35-40, col 18, lines 58-64).

For claim 511 (col 18, lines 25-29).

For claims 512 ,565 all operand stack and variables are stored in the same register file (col 16, lines 64-67, col 17, lines 1-10), and the operand stack and the variables are stored separately in the same register files is shown in (col 10 lines 45-54).

For claims 513, 566 (col 8, lines 25-32), where “virtual machine instruction” is the stack-based instruction.

For claims 514, 548,567, 596, (col 3, lines 23-30) and (col 3, lines 40-43), where “removes virtual machine instructions from the instruction buffer” is “flushing”.

For claims 515, 597, (col 10, lines 45-62), via at least one of the overflow and underflow mechanism (col 18, lines 25-29).

For claims 516, 550, 569, 598 (col 17, lines 10-40), via at least one of the overflow and underflow mechanism (col 18, lines 25-29).

For claims 517, 570 (col 18, lines 39-40, “In the exemplary embodiment of FIG. 1, memory includes data cache”).

For claims 519, 572 (col 17, lines 18-24).

For claims 520, 573, (col 2, lines 58-67).

For claims 521, 574, (col 28, lines 53-56, col 9, lines 10-17).

For claims 522,575, (Abstract), where hardware processor is the virtual machine (col 2 lines 59-60).

For claims 523,576 (col 10, lines 45-65).

For claims 524, 577, m(col 4, lines 20-26).

For claims 525, 578(col 4, lines 20-26, col 10, lines 4-10).

For claims 526, 546, 579, 594, (col 10, lines 45-65).

For claims 527, 549, 580(col 10, lines 5-15).

For claims 528,581, (col 10, lines 5-15).

For claims 529, 582, (col 10, lines 5-15).

For claim 530,

- decoding instruction ... set (col 3, lines 20-30)
- maintaining an operand stack ... underflow mechanism (col 3, line 64, col 18, lines 29-57, col 17, lines 10-15)
- decoding instruction ... set (col 3, lines 20-30, col 3, lines 40-43)
- maintaining data ... register file (col 3, lines 63-65)
- sending an output ... unit (col 18, lines 7-12)
- processing the output in the execution unit... virtual machine (col 18 lines 7-12, col 3 lines 40-42, col 3 lines 60-65)

For claims 531,584 (Abstract).

For claim 532, (col 3, lines 40-45).

For claims 533,586 (col 13, lines 11-19).

For claims 534, 587 (col 13 lines 20-35).

For claims 535, 588(col 16 lines 1-10).

For claim 536, (col 16 lines 1-10).

For claim 537, (col 3, lines 23-30).

For claims 538, 590, (col 10, lines 45-62, col 18, lines 25-29).

For claims 539, 591 (col 18, lines 39-40).

For claim 540,

- switching a processing system to an accelerator (col 22, lines 18-35), wherein stack-based instructions are executed directly in hardware (col 5, lines 36-46)
- generating an exception ... accelerator mode (col 22, lines 28-40, col 23, lines 56-64)
- switching the process ... virtual machine (col 21, lines 56-64, col 22 lines 12-18).

For claim 543

- processing instruction of a plurality of instruction sets in a CPU having an execution unit (Abstract, col 5 lines 36-48) and a register file (col 17, lines 11-15)
- wherein at least one of the plurality ... register-based instruction set (col 17, lines 32-39, col 17, lines 11-16)
- using a common program counter ... common register (col 10,lines 5-10)

- generating a branch taken signal ... sets (col 17, lines 18-24).

For claim 544, (col 10, lines 5-10).

For claim 545, (col 10, lines 5-10).

For claim 551, (col 5, lines 35-45, col 5, lines 43-45, abstract, col 3, lines 53-56, col 17, lines 32-39, col 17, lines 11-16, col 3 line 64, col 21 lines 57-62, col 6 lines 25-27). Tremblay discloses N-way switch system (col 21 lines 58-60), which shows the system can switch from one state to another state, encountering exception (col 23 lines 56-65).

For claims 552 ,553 (col 21 lines 58-60, col 23 lines 56-65).

For claim 555, col 21, lines 48-65.

For claim 556, (abstract).

For claim 557, col 21 lines 48-65.

For claim 559 (abstract, col 5 lines 43-45, col 3 lines 53-56, col 17 lines 32-39, col 17 lines 11-16 col 3 line 64, col 18 lines 29-57, col 9 lines 20-25, col 3 lines 39-42).

For claim 560 (col 9 lines 55-58, col 3 lines 23-30, col 17 lines 20-30).

For claim 561, (col 21 lines 48-55).

For claim 568, (col 10, lines 45-62, col 18, lines 25-29).

For claim 583 (abstract, col 5 lines 43-45, col 3 lines 53-56, col 17 lines 32-39, col 17 lines 11-16, col 3 lines 64-67, col 18 lines 29-57, col 17 lines 10-15, col 9 lines 20-25, col 3 lines 39-42, col 21 lines 48-60).

For claim 585 (col 9 lines 20-25).

For claim 589 (col 3, lines 20-30, col 3, lines 64-67, col 18, lines 29-57, col 17 lines 10-15, col 18 lines 7-12).

For claim 592, see the rejection of claims 551-557, 506, 539.

For claim 593, see the rejection of claims 506.

For claim 599, see the rejections of claims **551-557, 506, 539.**

For claims 600-654, see the rejection of claims 551-554.

For claim 606, col 23 lines 55-65.

For claim 607, col 22 lines 1-65.

For claim 609, col 21 lines 48-65.

For claim 610, col 16 lines 1-20.

For claim 611, col 16 lines 1-65.

For claim 612, col 16 lines 1-20.

For claim 613, col 15 lines 1-65.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 518, 547, 571, 595, 614, 615 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay, US 6,125,439 and further in view of official notice taken by the Examiner.

As per claims 518, 547, 571 Tremblay does not specifically disclose all the groups in the branch instructions. However, official notice is taken for all the groups in the branch instruction. The modification would be obvious because one of the ordinary skill in the art would be motivated to execute the instructions efficiently.

As per claims 614 and 615, Tremblay discloses lookupswitch, getfield, putfield method. Tremblay does not specifically disclose all other instructions in the limitations of claims 614 and 615. However, official notice is taken for all other instructions for generating the exception. The modification would be obvious because one of the ordinary skill in the art would be motivated to execute the instructions efficiently.

Conclusion

7. The prior art made or record and not relied upon is considered pertinent to applicant's disclosure.

TITLE: Virtualshadow registers and virtual register windows, US 6799269 B2

TITLE: Method and system for translating a non-native bytecode to a set of codes native to a processor within a computer system, US 5875336 A

TITLE: System with wide operand architecture, and method, US 6725356 B2

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chameli C. Das whose telephone number is (571) 272-3696. The examiner can normally be reached on 7-3:30 and examiner's supervisor Tuan Dam can be reached at (571) 272-3695.

An inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is 703-305-9600.

Chameli C Das
CHAMELI C. DAS 149/06,
PRIMARY EXAMINER